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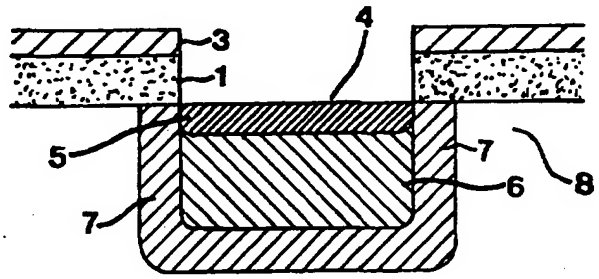
(54) Title: A METHOD FOR PRODUCING A CHANNEL REGION LAYER IN A SiC-LAYER FOR A VOLTAGE CONTROLLED SEMICONDUCTOR DEVICE

(57) Abstract

In a method for producing a channel region layer (3) in a Sic-layer (2) for producing a voltage controlled semiconductor device n-type dopants and p-type dopants are implanted into a surface-near layer (5) of the SiC layer. The p-type dopants implanted have a higher diffusion rate in SiC than the n-type dopants implanted. The SiC-layer is then heated at such a temperature that p-type dopants implanted diffuse from said surface-near layer into the surrounding regions of the SiC-layer being lightly n-doped to such a degree that a channel region layer in which p-type dopants dominates is created.



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A method for producing a channel region layer in a SiC-layer for a voltage controlled semiconductor device

TECHNICAL FIELD OF THE INVENTION AND PRIOR ART

The present invention relates to a method for producing a doped p-type channel region layer having on laterally opposite sides thereof doped n-type regions in a SiC-layer for producing a voltage controlled semiconductor device, as well as a voltage controlled semiconductor device produced by using such a method.

Such a method may be used for producing any voltage controlled semiconductor device, such as for instance MISFETs, MOSEFETs and IGBTs. This type of semiconductor devices of SiC may especially be used as switching devices in power applications owing to the possibility to turn them on and off very rapidly. Such devices made of SiC are particularly well suited for high power applications, since such applications make it possible to benefit from the superior properties of SiC in comparison with especially Si, namely the capability of SiC to function well under extreme conditions. This properties involving a high thermal stability, a high thermal conductivity and a high breakdown voltage are well known in the art, but another well known feature of SiC, namely the extremely low diffusivity of dopants at convenient temperatures therein, has until now made it very difficult to produce a channel region layer, especially having a narrow width, for a voltage controlled semiconductor device of SiC in a simple and reliable manner. For for instance Si there

will be no problem to produce such channel region layers, since the diffusion technique functions excellent for Si.

SUMMARY OF THE INVENTION

The object of the present invention is to provide a method of the type defined in the introduction, which makes it possible to produce a channel region layer in a voltage controlled semiconductor device of SiC in a simple and thereby commercially interesting way.

This object is according to the invention obtained by providing such a method with the steps of:

1) applying a masking layer on top of a SiC-layer being lightly n-doped,

2) etching an aperture in said masking layer extending to the SiC-layer,

3) implanting n-type dopants into an area of said SiC-layer defined by said aperture for obtaining a high doping concentration of n-type in a surface-near layer of the SiC-layer under said area,

4) implanting p-type dopants having a considerably higher diffusion rate in SiC than the n-type dopants implanted in step 3) into an area of the SiC-layer defined by said aperture to such a degree that the doping type of said surface-near layer created by carrying out step 3) is maintained,

5) heating said SiC-layer at such a temperature that p-type dopants implanted in step 4) in said surface-near layer diffuse into the surrounding regions of the SiC-layer being lightly n-doped to such a degree that a

channel region layer in which p-type dopants dominates is created laterally to said highly doped n-type surface-near layer and between this layer and lightly n-doped regions of the SiC-layer,

said p-type dopants being implanted in step 4) to such a degree that the doping type in the lightly n-doped regions closest to said highly doped n-type surface-near layer may be shifted to p-type through diffusion of said p-type dopants, and wherein the steps 3) and 4) are carried out in one of a) the order mentioned and b) first step 4) and then step 3).

Accordingly, the invention is based on the understanding that the diffusion technique may after all be used also for SiC to create a channel region layer having a width easily controlled and which may be made very narrow when decided. Thus, the invention utilises the fact that some acceptors have a substantially higher diffusion rate in SiC than donors, which do almost not diffuse in SiC at all. By implanting dopants of different doping types in said surface-near layer and heating this layer p-type dopants will diffuse out thereof for forming said channel region layer while the n-type dopants implanted will stay in said surface-near layer. It is apparent to those skilled in the art that the width of the channel region layer produced in this way may be easily controlled by controlling the time period during which it is heated and the temperature at which it is heated in step 5). Thus, such a channel region layer may be given any width, and very short channels resulting in the lower on-state resistance of the device may in this way be easily obtained without any requirement of any delicate process steps of a very high accuracy, since the channel is not defined by lithography.

According to a preferred embodiment of the invention the implantation in step 3) is carried out to different depths into said SiC-layer defined by said aperture, so that p-type dopants are implanted deeply into said area for creating a deep layer of p-type under said surface-near layer of n-type created in step 3). It will in this way by such deep implantation be possible to create a device having a DMOS-type of structure in SiC. A more appropriate name for such a device would be a VIMOS (a vertical implanted MOS), but it is emphasised that this embodiment also of course covers the case of producing other type of voltage controlled semiconductor devices of SiC having a deeply implanted layer, such as for instance IGBTs.

According to another preferred embodiment of the invention boron is implanted as p-type dopant in step 4). The diffusion rate of boron in SiC is comparatively high for SiC circumstances, since boron has rather small atoms, at annealing temperatures being not that high, so that said channel region layer may by using boron as said dopant be easily created in a commercially interesting period of time without any necessity of exaggeratedly the high heating temperatures, but an annealing temperature in the order of 1 700°C for making the dopants implanted will do well.

According to another preferred embodiment of the invention beryllium is implanted as p-type dopant in step 4). Beryllium has nearly the same diffusivity in SiC as boron, but it has a severe disadvantage of being highly toxic.

According to another very preferred embodiment of the invention the masking layer is applied in step 1) by applying an insulating layer of AlN on top of the SiC-layer and a layer of a refractory material being a conductor of electricity on top of the AlN-layer, and these two layers are left on the SiC-layer during step 5) for forming the gate insulating

layer and the gate electrode, respectively, of the voltage controlled semiconductor device produced by using this method. By using AlN as material for the gate insulating layer and a refractory material as gate electrode, the preferred self-alignment technique may be used to produce the device, so that a gate electrode will be self-aligned with respect to the border of said channel region layer to the highly doped n-type surface-near layer. Such a method will include very few masking steps and by that be commercially very competative.

According to a preferred further development of the embodiment last mentioned TiN is applied in step 1) on top of said insulating layer for forming the layer for said gate electrode. The use of TiN as a refractory metal for said gate is advantageous, since TiN forms a stable interface with AlN, and these two materials may without any problem withstand the high temperatures necessary for carrying out the step of diffusion in SiC.

The invention also comprises a method for producing a voltage controlled semiconductor device of SiC, being one of a) a MISFET and b) an IGBT, comprising the steps of:

6) epitaxially growing on top of each other the following semiconductor layers of SiC: a highly doped substrate layer being for a) of n-type and for b) of p-type, for b) on top thereof one of c) a highly doped n-type buffer layer and d) no such layer, and a low doped n-type drift layer,

this method is characterized in that it also comprises the following steps:

7) carrying out the steps according to claims 1, 3 and 11 and/or 12 according to one of the two orders defined in claim 1 for forming a doped n-type source region layer, a doped p-type base layer located thereunder and a doped p-type channel region layer,

8) depositing a source in contact with said highly doped n-type source region layer,

9) applying a passivation layer on top of the layers of the device,

10) etching an aperture through the passivation layer to said gate electrode and applying means for an external contact thereto.

Such a method is very advantageous, since it comprises very few masking steps, namely only four such steps, which is a very low number for the production of semiconductor devices of this type. It is in fact the number of masking steps that to a large extent determines the production costs of a semiconductor component, since the material constitutes a neglectable part of the costs. Accordingly, this method is very preferred and is well suited for commercially production of voltage controlled semiconductor devices of SiC.

According to another preferred embodiment of the invention this method also comprises a step of etching a groove through said highly doped n-type source region layer and into the p-type base layer located thereunder, this step is carried out before step 8) and said source is deposited in the groove for forming a contact to both said p-type base layer and said n-type source region layer. It is preferred to arranged the source into contact with the base layer in this way so as to stabilise the device against potential fluctuations.

The invention also involves voltage controlled semiconductor devices of SiC produced by a method comprising the steps according to any of the appended method claims. The advantages of such devices will clearly appear from above.

Further advantages and preferred features of the invention will appear from the description and the other dependent claims.

BRIEF DESCRIPTION OF THE DRAWING

With reference to the appended drawing, below follows a specific description of a preferred embodiment of the invention cited as an example.

In the drawings:

Fig. 1 and 2 are schematic cross-section views illustrating the two main steps of a method for producing a channel region layer in a SiC-layer for producing a voltage controlled semiconductor device according to a preferred embodiment of the invention, and

Fig. 3 is a schematic cross-section view illustrating how the voltage controlled semiconductor device produced by utilising the method steps illustrated in Figs. 1 and 2 and further conventional processing steps may look like.

DETAILED DESCRIPTION OF A PREFERRED EMBODIMENT OF THE INVENTION

A method for producing a channel region layer in a SiC-layer for producing a voltage controlled semiconductor device will

now be described with reference to Figs. 1 and 2. Conventional semiconductor device producing steps having nothing to do with the invention have for the sake of clearness not been shown in the figures. First of all an insulating layer 1 of AlN is applied on top of a SiC-layer 2 being lightly n-doped preferably at a doping concentration of about 10^{15} cm^{-3} with a suitable donor, such as for instance N or P. The SiC-layer is monocrystalline, and due to the good lattice-match of monocrystalline AlN with SiC the AlN-layer may be applied on the SiC-layer while obtaining a high interface quality between the layers 1 and 2 by for instance CVD. A further layer 3 of a refractory material being a conductor of electricity, in this case TiN, is applied on top of the AlN-layer. An aperture 4 is then etched through the layers 1 and 3 and to the surface of the SiC-layer 2. n-type dopants are then implanted into an area of the SiC-layer defined by said aperture for forming a high doping concentration of donors in a surface-near layer 5 of the SiC-layer under said area. Any type of donors suitable for SiC may be used, such as for instance N and P. After that p-type dopants having a considerably higher diffusion rate in SiC than the n-type dopants implanted for forming the layer 5 are implanted into the area of the SiC-layer defined by said aperture to such a degree that the doping type of said surface-near layer is maintained, i.e. the donors do still dominate in this layer. The implantation of the p-type dopants are carried out to different depths, i.e. while using different acceleration energies therefor, into said SiC-layer, so that p-type dopants are implanted deeply into this area when high energies, such as 300 keV, are used for creating a deep layer 6 of p-type under the layer 5. This implantation is preferably carried out so that the layer 6 will be highly doped. Acceptors having a reasonable high diffusion rate in SiC are boron, beryllium and aluminium. Boron is the preferred one, since beryllium is highly toxic and aluminium requires temperatures of about 2 000°C for obtaining a

reasonable diffusion rate, whereas the corresponding temperature for boron is about 1 700°C.

Said SiC-layer is then heated at such a temperature that p-type dopants implanted in the layers 5 and 6 diffuse into the surrounding regions of the SiC-layer being lightly n-doped to such a degree that a layer 7 surrounding the layers 5 and 6 and in which p-type dopants dominates is created. Accordingly a channel region layer 7 is in this way created laterally to the layer 5 and between this layer and lightly n-doped regions 8 of the SiC-layer. Accordingly, it is important that the p-type dopants are implanted in at least said surface-near layer 5 to such a degree that the doping type in the lightly n-doped regions closest to said highly doped n-type surface-near layer 5 may be shifted to p-type through diffusion of said p-type dopants. Accordingly, the doping concentration of the acceptors in the layer 5 may be chosen to be for example 10^{17}-$10^{18}cm^{-3}$. The channel region layer 7 will be lightly p-doped. The width of the channel region layer may be controlled by selecting the temperature at which it is heated and the period of time for said heating, so that very narrow channel region layers may in this way be obtained if desired. Due to the fact that AlN and the layer 3 of a refractory material are used as a masking layer for the implantation the masking layer may be left there during the heating, since they withstand the high temperatures used, so that the insulating layer 1 and the layer 3 may be left as the gate insulating layer and the gate electrode, respectively, in the voltage controlled semiconductor device produced in this way minimising the masking steps required. Thanks to this fact the gate electrode 3 will also be self-aligned with respect to the surface-near layer 5 forming a source region layer with no overlap.

However, it is emphasised that it is well possible to use for instance an oxide as insulating layer in a device pro-

duced by using the inventional method, in which case the insulating layer may not be there during the diffusion step and no self-alignment will be obtained, although the self-alignment technique shown in Figs. 1 and 2 will be preferred thanks to the very few masking steps resulting therefrom. Thus, the key of the present invention is that it is utilised that donors do practically not at all diffuse in SiC but some acceptors do, for forming a channel region layer.

After the heating step a groove 9 (see Fig. 3) is etched through the layer 5 and into the layer 6 thereunder, whereupon a source 10 is deposited in contact with the source region layer 5 and the base layer 6. A suitable passivation layer not shown in the figures is after that applied on top of the layers of the device, and an aperture is finally etched through the passivation layer to said gate electrode 3 and means 11 for an external contact thereto are applied.

The entire process for producing a voltage controlled semiconductor device, which in this case is an IGBT, is started by epitaxially growing on top of each other the following semiconductor layers of SiC: A highly doped substrate layer 12 of p-type, a highly doped n-type buffer layer 13 and a low doped n-type drift layer 14. A drain 15 is applied in contact with the substrate layer 12. A MISFET may be produced in the same way but without the highly doped p-type layer 12. In the case of a MISFET this may be said to be a VIMIS (vertical implanted MIS) having a similar construction as a DMOS in Si. Actually, two IGBTs produced in this way connected in parallel are shown in Fig. 3.

Typical dimensions for a device producable in this way are: width of channel region layer 0,3 μm, width of source region layer 0,2 μm and depth of base layer 0,7 μm.

The invention is of course not in any way restricted to the preferred embodiment described above, but many possibilities to modifications thereof will be apparent to a man skilled in the art without departing from the basic idea of the invention.

It is emphasised that the thicknesses of different layers in the figures cannot be interpreted as limiting the scope of the protection, but any thickness relations are intended to be covered by the claims.

The number of layers mentioned in the claims is a minimum number, and it is within the scope of the invention to arrange further layers in the device or dividing any layer into several layers by selective doping of different regions thereof. It is not necessary that a deep implantation of p-type dopants takes place, but it will be sufficient for forming said channel region layer that p-type dopants are implanted into a surface-near region of the SiC layer and after that the heating is carried out for diffusion of the dopants out thereof for forming a channel region layer laterally to the highly doped n-type surface-near layer.

"Substrate layer" is in this disclosure to be interpreted as the layer closest to the drain of the layers mentioned and it has not to be a substrate layer in the strict sense of this word within this field, i.e. the layer from which the growth is started. The real substrate layer may be any of the layers and it is mostly the thickest one.

The layers located on top of each other does not have to be epitaxially grown in the order they are mentioned in the claims, but any other order of growth of these layers is within the scope of the claims. For instance the growth may be started from the drift layer and the so called substrate

layer and the drain may be grown at the very end of the method or conversely.

Claims

1. A method for producing a doped p-type channel region layer having on laterally opposite sides thereof doped n-type regions in a SiC-layer for producing a voltage controlled semiconductor device, comprising the steps of:

1) applying a masking layer (1, 3) on top of a SiC-layer (2) being lightly n-doped,

2) etching an aperture (4) in said masking layer extending to the SiC-layer,

3) implanting n-type dopants into an area of said SiC-layer defined by said aperture for obtaining a high doping concentration of n-type in a surface-near layer (5) of the SiC-layer under said area,

4) implanting p-type dopants having a considerably higher diffusion rate in SiC than the n-type dopants implanted in step 3) into an area of the SiC-layer defined by said aperture to such a degree that the doping type of said surface-near layer created by carrying out step 3) is maintained,

5) heating said SiC-layer at such a temperature that p-type dopants implanted in step 4) in said surface-near layer (5) diffuse into the surrounding regions of the SiC-layer being lightly n-doped to such a degree that a channel region layer (7) in which p-type dopants dominates is created laterally to said highly doped n-type surface-near layer and between this layer and lightly n-doped regions (8) of the SiC-layer,

said p-type dopants being implanted in step 4) to such a degree that the doping type in the lightly n-doped regions

closest to said highly doped n-type surface-near layer may be shifted to p-type through diffusion of said p-type dopants, and wherein the steps 3) and 4) are carried out in one of a) the order mentioned and b) first step 4) and then step 3).

2. A method according to claim 1, characterized in that it comprises a step carried out after step 4) and before step 5) of removing said masking layer by etching.

3. A method according to claim 1 or 2, characterized in that the implantation in step 3) is carried out to different depths into said SiC-layer (2) defined by said aperture (4), so that p-type dopants are implanted deeply into said area for creating a deep layer (6) of p-type under said surface-near layer (5) of n-type created in step 3).

4. A method according to any of claims 1-3, characterized in that boron is implanted as p-type dopant in step 4).

5. A method according to any of claims 1-4, characterized in that beryllium is implanted as p-type dopant in step 4).

6. A method according to any of claims 1-5, characterized in that the heating in step 5) is carried out at such a temperature that the dopants implanted in step 3) and 4) are made electrically active.

7. Method according to claim 4, characterized in that said heating in step 5) is carried out at a temperature above 1 650°C.

8. Method according to claim 7, characterized in that said heating in step 5) is carried out at a temperature below 1 800°C.

9. A method according to any of claims 1-8, characterized in that the width of the channel region layer (7) is controlled by controlling the time period during which it is heated and the temperature at which it is heated in step 5).

10. A method according to claim 3, characterized in that said deep layer is created by using energies above 200keV for the implantation in step 4).

11. A method according to any of claims 1 and 3-10, characterized in that the masking layer is applied in step 1) by applying an insulating layer (1) of AlN on top of the SiC-layer (2) and a layer (3) of a refractory material being a conductor of electricity on top of the AlN-layer, and that these two layers are left on the SiC-layer during step 5) for forming the gate insulating layer and the gate electrode, respectively, of the voltage controlled semiconductor device produced by using this method.

12. A method according to claim 11, characterized in that TiN is applied in step 1) on top of said insulating layer (1) for forming the layer for said gate electrode.

13. A method for producing a voltage controlled semiconductor device of SiC, being one of a) a MISFET and b) an IGBT, comprising the steps of:

6) epitaxially growing on top of each other the following semiconductor layers of SiC: a highly doped substrate layer (12) being for a) of n-type and for b) of p-type, for b) on top thereof one of c) a highly doped n-type buffer layer (13) and d) no such layer, and a low doped n-type drift layer (14),

characterized in that it also comprises the following steps:

7) carrying out the steps according to claims 1, 3 and 11 and/or 12 according to one of the two orders defined in claim 1 for forming a highly doped n-type source region layer (5), a doped p-type base layer (6) located thereunder and a doped p-type channel region layer (7),

8) depositing a source (10) in contact with said highly doped n-type source region layer,

9) applying a passivation layer on top of the layers of the device,

10) etching an aperture through the passivation layer to said gate electrode (3) and applying means (11) for an external contact thereto.

14. A method according to claim 13, characterized in that it also comprises a step of etching a groove (9) through said highly doped n-type source region layer (5) and into the p-type base layer (6) located thereunder, that this step is carried out before step 8), and that said source (10) is deposited in said groove for forming a contact to both said p-type base layer and said n-type source region layer.

15. A voltage controlled semiconductor device of SiC produced by a method comprising the steps according to any of claims 1-14.

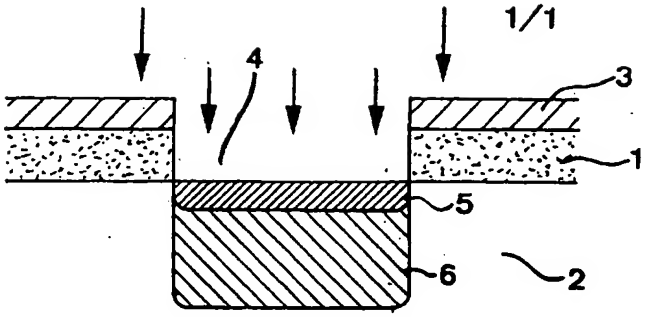

Fig 1

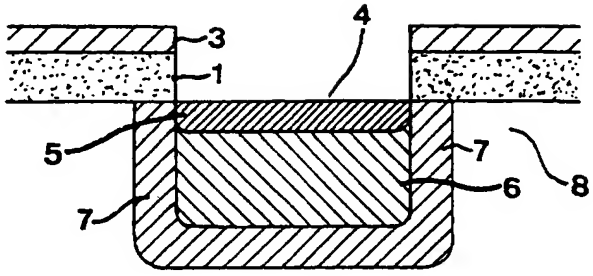

Fig 2

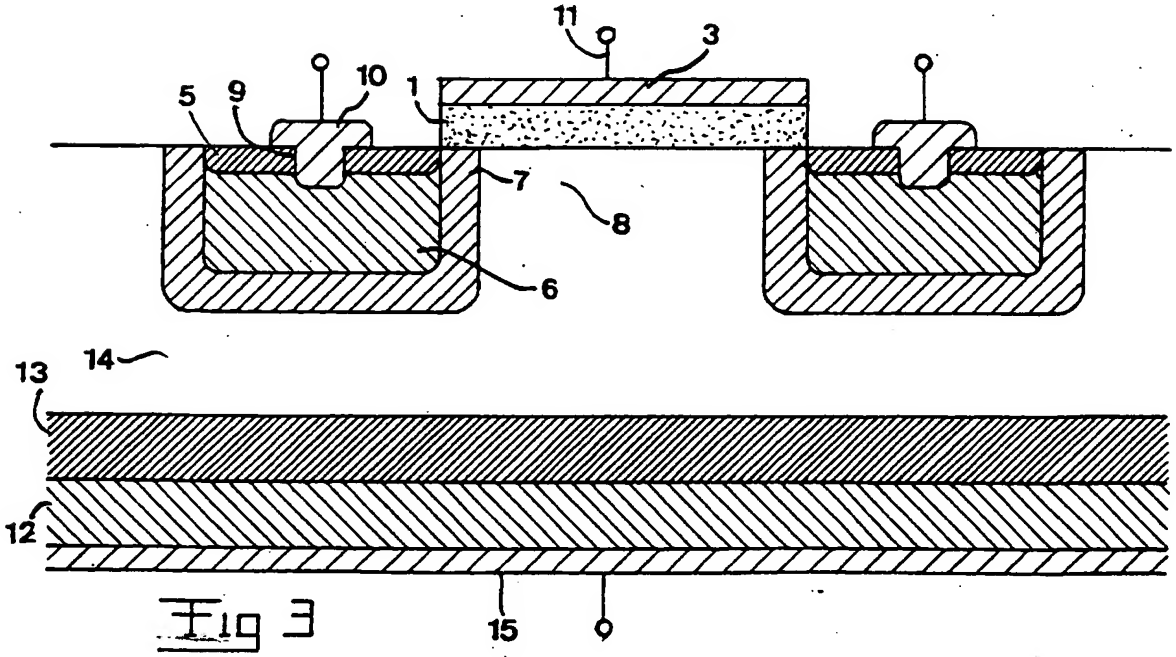

Fig 3

INTERNATIONAL SEARCH REPORT

International application No.
PCT/SE 97/01002

A. CLASSIFICATION OF SUBJECT MATTER

IPC6: H01L 21/335, H01L 29/24, H01L 21/22, H01L 21/265
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

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Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

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Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

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C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5348895 A (MICHAEL C. SMAYLING ET AL), 20 Sept 1994 (20.09.94), column 1, line 57 - column 3, line 13, claims 1-19	1-10,15
A	--	11-14
A	WO 9619834 A2 (ABB RESEARCH LTD.), 27 June 1996 (27.06.96), page 6, line 22 - page 7, line 22, figures 1,4, abstract	11-14
A	--	11-14
A	US 4570328 A (J. B. PRICE ET AL), 18 February 1986 (18.02.86), column 1, line 51 - column 2, line 5, figures 2-5, abstract	12-14
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☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
16 October 1997	20 -10- 1997
Name and mailing address of the ISA/ Swedish Patent Office Box 5055, S-102 42 STOCKHOLM Facsimile No. +46 8 666 02 86	Authorized officer Stig Edhborg Telephone No. +46 8 782 25 00

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Information on patent family members

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International application No.
PCT/SE 97/01002

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